Plasma CVD and ALD processes for non-volatile resistive memories and for selective deposition processes

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With this presentation I will address some recent research obtained in LTM (Laboratory of Technology de la Microelectronic (LTM), Grenoble Alpes University).

First, I will talk about Dual Frequency (DF) PECVD processes for Phase Change Material (GeSbTe) deposition. For this study we used a 200 mm commercial PECVD tool from Altatech with a pulsed liquid injection of precursors. I will show that a very strong improvement of the gap filling capability of the process is obtained by using the DF mode.

I will then talk about HfO_2 for Resistive RAM. Resistive switching is a phenomenon by which some electrical insulators display a change of resistance upon application of a bias voltage. I will show that the electrical characterization of the MIM in two electrical modes, voltage sweep mode and constant voltage stress (CVS) mode, can be very useful to understand the mechanisms of the resistance switching. I will also show that a double layer can be introduced in the MIM stacks to achieve a new type of device called Mem-impedance.

The last part of this talk will be dedicated to the development of a selective deposition process by PEALD. One of the main challenges brought by the reduction of the transistor size below 10 nm is the development of selective deposition processes. ALD is a suitable technique for selective deposition since it is a self-limited surface reaction process. I will show that using both PEALD and ALE (Atomic Layer Etching) one deposit selectively Ta_2O_5 oxide on top of metal (TiN) while no deposition is obtained on Si or SiO_2 surfaces.